IN THE CLAIMS

1. (Currently Amended) A delay locked loop (DLL) comprising:

a delay line including an input for receiving an external clock signal, and multiple outputs for providing multiple delayed signals including a first delayed signal and a second delayed signals;

a selector connected to the multiple outputs for selecting ~~one of~~ the first delayed signal ~~the multiple delayed signals as~~ to provide an internal clock signal such that the external and internal clock signals are synchronized ~~, wherein the multiple delayed signals have different delays in relation to the external clock signal~~; and

a command react circuit connected to the selector~~, the command react circuit capable of activating a command set signal~~ for enabling the selector to select ~~a different~~ the second delayed signal ~~among the multiple delayed signals~~ based on a first state of a command signal to provide the internal signal ~~while the external and internal clock signals are synchronized~~ and for enabling the selector to select the first delayed signal based on a second state of the command to provide the internal signal.

2. (Original) The DLL of claim 1 further comprising:

a phase detector for comparing the external and internal clock signals to produce shifting signals; and

a controller connected to the delay line for adjusting an amount of delay applied to the external clock signal based on the shifting signals when the external and internal clock signals are not synchronized.

3. (Original) The DLL of claim 1, wherein delay line includes a plurality of delay stages connected in series, wherein one of the multiple outputs connects to an output of the next to last delay stage, wherein another output of the multiple outputs connects to an output of the last delay stage.

4. (Original) The DLL of claim 1, wherein the selector includes a multiplexor, the multiplexor including a plurality of inputs to receive the multiple delay signals and an output to provide the internal clock signal.

5. (Currently Amended) The DLL of claim 1, wherein the command react circuit includes:

a first input for receiving the command signal from the phase detector;

a second input for receiving a phase detect signal, wherein the phase detector is configured to deactivate the phase detect signal ~~being deactivated~~ when the external and internal clock signals are not synchronized; and

an output for providing the command set signal, wherein the command react circuit is configured to activate the command set signal ~~is activated~~ when the command signal is activated to enable the selector to select ~~a different one of~~ the second delayed signal[[s]] before the phase detect signal is deactivated.

6. (Currently Amended) A delay locked loop (DLL) comprising:

a plurality of delay stages for applying a first amount of delay to an external signal to generate a first delayed signal and for applying a second amount of delay to ~~an~~ the external clock signal to generate a second delayed signal;

a selector connected to the delay stages for receiving the first and second delayed ~~signal~~ signals to provide an internal clock signal such that the external and internal clock signals are synchronized; and

a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal [[and]] , a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable ~~wherein the command react circuit causes~~ the selector to ~~select~~ provide the internal signal based on [[a]] the second ~~amount of delay~~ delayed signal when the command signal is activated ~~while the external and internal clock signals are synchronized~~, and to provide the internal signal based on the first delayed signal when the command signal is deactivated.

7. (Currently Amended) The DLL of claim 6, wherein the command react circuit ~~causes~~ is configured to enable the selector to select the first ~~amount of delay~~ delayed signal when the phase detect signal is activated and the command signal is not activated.

8. (Original) The DLL of claim 6 further comprising:

a phase detector for comparing the external and internal clock signals to produce shifting signals; and

a controller connected to the delay stages for adjusting the first and second amount of delays based on the shifting signals when the external and internal clock signals are not synchronized.

9. (Currently Amended) The DLL of claim 6, wherein the plurality of delay stages are configured to apply the first amount of delay [[is]] greater than the second amount of delay.

10. (Currently Amended) The DLL of claim 6, wherein the plurality of delay stages are configured to apply the first amount of delay [[is]] smaller than the second amount of delay.

11. (Currently Amended) The DLL of claim 6, wherein the plurality of delay stages are configured to apply the first and second amount of delays in which a difference between the first and second amount of delays is equaled to a predetermined delay.

12. (Currently Amended) The DLL of claim 6 further comprising a phase detector connected to the command react circuit to provide the phase detect signal, and wherein the phase detector is configured to activate~~, wherein~~ the phase detect signal ~~is activated~~ when the external and internal clock signals are not synchronized.

13. (Currently Amended) A delay locked loop (DLL) comprising:

a plurality of delay stages for applying a first amount of delay to an external signal to generate a first delayed signal and for applying a second amount of delay to ~~an~~ the external clock signal to generate a second delayed signal, wherein the second amount of delay is smaller than the first amount of delay by a delay quantity;

a selector connected to the delay stages for receiving the first and second delayed ~~signal~~ signals to provide an internal clock signal such that the external and internal clock signals are synchronized; and

a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal [[and]] , a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable ~~wherein the command react circuit causes~~ the selector to ~~select~~ provide the internal signal based on [[a]] the second ~~amount of delay~~ delayed signal ~~smaller than the first amount of delay by a delay quantity~~ when the command signal is activated ~~while the external and internal clock signals are synchronized~~, and to provide the internal signal based on the first delayed signal when the command signal is deactivated.

14. (Currently Amended) The DLL of claim 13, wherein the command react circuit ~~causes~~ is configured to enable the selector to select the first ~~amount of delay~~ delayed signal when the phase detect signal is activated and the command signal is not activated.

15. (Currently Amended) The DLL of claim 13 further comprising:

a phase detector for comparing the external and internal clock signals to produce shifting signals; and

a shift register for adjusting the ~~amount of delays~~ first amount of delay and the second amount of delay based on the shifting signals when the external and internal clock signals are not synchronized.

16. (Original) The DLL of claim 13, wherein the selector includes a multiplexor.

17. (Currently Amended) The DLL of claim 13, wherein the plurality of delay stages are configured to provide the delay quantity [[is]] equaled to a delay of at least one delay stage.

18. (Currently Amended) The DLL of claim 13, wherein the delay quantity is equaled to a predetermined delay.

19. (Currently Amended) The DLL of claim 13 further comprising a phase detector connected to the command react circuit to provide the phase detect signal, and wherein the phase detector is configured to activate~~, wherein~~ the phase detect signal ~~is activated~~ when the external and internal clock signals are not synchronized.

20. (Currently Amended) The DLL of claim [[13]] 19, wherein the command react circuit further including a third input for receiving a phase lock signal from the phase detector, and wherein the phase detector is configured to activate[[,]] the phase lock signal ~~being activated~~ when the external and internal clock signals are synchronized.

21. (Currently Amended) The DLL of claim 20, wherein the command react circuit ~~causes~~ is configured to enable the selector to select the first ~~amount of delay~~ delayed signal when the phase lock signal is activated and the command signal is not activated.

22. (Currently Amended) A delay locked loop (DLL) comprising:

a plurality of delay stages for applying a first amount of delay to an external signal to generate a first delayed signal and for applying a second amount of delay to ~~an~~ the external clock signal to generate a second delayed signal, wherein the second amount of delay is greater than the first amount of delay by a delay quantity;

a selector connected to the delay stages for receiving the first and second delayed ~~signal~~ signals to provide an internal clock signal~~, wherein~~ such that the external and internal clock signals are synchronized; and

a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal [[and]] , a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable ~~wherein the command react circuit~~ ~~causes~~ the selector to ~~select~~ provide the internal signal based on [[a]] the second ~~amount of delay~~ delayed signal ~~smaller than the first amount of delay by a delay quantity~~ when the command signal is activated ~~while the external and internal clock signals are synchronized~~, and to provide the internal signal based on the first delayed signal when the command signal is deactivated.

23. (Currently Amended) The DLL of claim 22, wherein the command react circuit ~~causes~~ is configured to enable the selector to select the first ~~amount of delay~~ delayed signal when the phase detect signal is activated and the command signal is not activated.

24. (Currently Amended) The DLL of claim 22 further comprising:

a phase detector for comparing the external and internal clock signals to produce shifting signals; and

a shift register for adjusting the ~~amount of delays~~ first amount of delay and the second amount of delay based on the shifting signals when the external and internal clock signals are not synchronized.

25. (Original) The DLL of claim 22, wherein the selector includes a multiplexor.

26. (Original) The DLL of claim 22, wherein delay quantity is equal to a predetermined delay.

27. (Currently Amended) The DLL of claim 22 further comprising a phase detector connected to the command react circuit to provide the phase detect signal, and wherein the phase detector is configured to activate~~, wherein~~ the phase detect signal ~~is activated~~ when the external and internal clock signals are not synchronized.

28. (Currently Amended) The DLL of claim [[22]] 27, wherein the command react circuit further including a third input for receiving a phase lock signal from the phase detector, and wherein the phase detector is configured to activate[[,]], the phase lock signal ~~being activated~~ when the external and internal clock signals are synchronized.

29. (Currently Amended) The DLL of claim 28, wherein the command react circuit ~~causes~~ is configured to enable the selector to select the first ~~amount of delay~~ delayed signal when the phase lock signal is activated and the command signal is not activated.

30. (Currently Amended) A delay locked loop (DLL) comprising:

a plurality of delay stages for ~~receiving~~ applying an amount of delay to an external clock signal to generate a first delayed signal and a second delayed signal;

a selector connected to the delay stages for selecting between the first and second delayed signals to [[be]] provide an internal clock signal~~, wherein the external and internal clock signals are synchronized~~; and

a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal [[and]] , a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable ~~wherein the command react circuit causes~~ the selector to replace the first delayed signal with the second delayed signal ~~as the internal signal~~ when the command signal is activated while the external and internal clock signals are synchronized and to enable the selector to replace the second delayed signal with the first delayed signal when the command signal is deactivated.

31. (Currently Amended) The DLL of claim 30, wherein the command react circuit ~~causes~~ is configured to enable the selector to replace the second delayed signal with the first delayed signal as the internal signal when the phase detect signal is activated and the command signal is not activated.

32. (Currently Amended) The DLL of claim 30 further comprising:

a phase detector for comparing the external and internal clock signals to produce shifting signals; and

a controller connected to the delay stages for adjusting the amount of ~~delays~~ delay based on the shifting signals when the external and internal clock signals are not synchronized.

33. (Currently Amended) The DLL of claim 30, wherein the plurality of delay stages are configured to provide the first delayed signal ~~is provided by~~ using a first number of delay stages, and the second delayed signal ~~is provided by~~ using a second number of delay stages, wherein the difference between the first and second number of delay stages is equal to a predetermined delay.

34. (Currently Amended) The DLL of claim 30, wherein the plurality of delay stages are configured to provide the first delayed signal ~~is provided by~~ using a first number of delay stages, and the second delayed signal ~~is provided by~~ using a second number of delay stages, wherein the first number of delay stages is greater than the second number of delay stages.

35. (Currently Amended) The DLL of claim 30, wherein the plurality of delay stages are configured to provide the first delayed signal ~~is provided by~~ using a first number of delay stages, and the second delayed signal ~~is provided by~~ using a second number of delay stages, wherein the first number of delay stages is less than the second number of delay stages.

36. (Currently Amended) The DLL of claim 30 further comprising a phase detector connected to the command react circuit to provide the phase detect signal, and wherein the phase detector is configured to activate~~, wherein~~, wherein the phase detect signal ~~is activated~~ when the external and internal clock signals are not synchronized.

37. (Currently Amended) The DLL of claim 30 further comprising a first delay output node and a second delay output node, wherein the plurality of delay stages are connected in series and include a common input to receive the external clock signal, wherein a last delay stage in the series of the delay stages includes an output node connected to the first delay output node to provide the first delayed signal ~~is generated at an output of the last delay stage in the series~~, and wherein a next to last delay stage in the series of the delay stages includes an output node connected to the second delay output node to provide the second delayed signal ~~is generated by an output of the next to last delay stage in the series~~.

38. (Currently Amended) The DLL of claim 30 further comprising a first delay output node and a second delay output node, wherein the plurality of delay stages are connected in series and include a common input to receive the external clock signal, wherein a last delay stage in the series of the delay stages includes an output node connected to the first delay output node to provide the first delayed signal ~~is generated at an output of the last delay stage in the series~~, and wherein another delay stage in the series of the delay stages includes an output node connected to

the second delay output node to provide the second delayed signal ~~is generated by an output of another delay stage in the series~~.

39. (Currently Amended) The DLL of claim [[30]] 36, wherein the command react circuit further comprising a third input for receiving a phase lock signal from the phase detector, and wherein the phase detector is configured to activate the phase lock signal ~~being activated~~ when the external and internal clock signals are synchronized.

40. (Currently Amended) The DLL of claim 39, wherein the command react circuit ~~causes~~ is configured to enable the selector to replace the second delayed signal with the first delayed signal as the internal signal when the phase lock signal is activated and the command signal is not activated.

41. (Currently Amended) A delay locked loop (DLL) comprising:

a plurality of delay stages for applying an amount of delay to an external clock signal to generate a first delayed signal and a second delayed signal;

a selector connected to the delay stages for selecting between the first and second delayed signals to [[be]] provide an internal clock signal~~, wherein the external and internal clock signals are synchronized~~;

a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal [[and]] , a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable ~~wherein the command react circuit causes~~ the selector to replace the first delayed signal with the second delayed signal ~~as the internal clock signal~~ when the command signal is activated while the external and internal clock signals are synchronized, ~~wherein the command react circuit causes~~ and to enable the selector to replace the second delayed signal with the first delayed signal ~~as the internal clock signal~~ when the phase detect signal is activated and the command signal is not activated;

a phase detector for comparing the external and internal clock signals to produce shifting signals; and

a controller connected to the delay stages for adjusting the amount of ~~delays~~ delay based on the shifting signals when the external and internal clock signals are not synchronized.

42. (Currently Amended) The DLL of claim 41, wherein the plurality of delay stages are configured to provide the first delayed signal ~~is provided by~~ using a first number of delay stages, and the second delayed signal ~~is provided by~~ using a second number of delay stages, wherein the difference between the first and second number of delay stages is equal to a predetermined delay.

43. (Currently Amended) The DLL of claim 41, wherein the plurality of delay stages are configured to provide the first delayed signal ~~is provided by~~ using a first number of delay stages, and the second delayed signal ~~is provided by~~ using a second number of delay stages, wherein the first number of delay stages is greater than the second number of delay stages.

44. (Currently Amended) The DLL of claim 41, wherein the plurality of delay stages are configured to provide the first delayed signal ~~is provided by~~ using a first number of delay stages, and the second delayed signal ~~is provided by~~ using a second number of delay stages, wherein the first number of delay stages is less than the second number of delay stages.

45. (Currently Amended) The DLL of claim 41, wherein the phase detector is configured to activate the phase detect signal ~~is activated~~ when the external and internal clock signals are not synchronized.

46. (Currently Amended) The DLL of claim 41 further comprising a first delay output node and a second delay output node, wherein the delays stages are connected in series and include a common input to receive the external clock signal, wherein a last delay stage in the series of the delay stages includes an output node connected to the first delay output node to provide the first delayed signal ~~is generated at an output of the last delay stage in the series~~, and wherein a next to last delay stage in the series of the delay stages includes an output node connected to the second delay output node to provide the second delayed signal ~~is generated by an output of the next to last delay stage in the series~~.

47. (Currently Amended) The DLL of claim 41, 30 further comprising a first delay output node and a second delay output node, wherein the plurality of delay stages are connected in series and include a common input to receive the external clock signal, wherein a last delay stage in the series of the delay stages includes an output node connected to the first delay output node to provide the first delayed signal ~~is generated at an output of the last delay stage in the series~~, and wherein another delay stage in the series of the delay stages includes an output node connected to the second delay output node to provide the second delayed signal ~~is generated by an output of another delay stage in the series~~.

48. (Currently Amended) The DLL of claim 41, wherein the command react circuit further comprising a third input for receiving a phase lock signal from the phase detector, and wherein the phase detector is configured to activate, the phase lock signal ~~being activated~~ when the external and internal clock signals are synchronized.

49. (Currently Amended) The DLL of claim 48, wherein the command react circuit ~~causes~~ is configured to enable the selector to replace the second delayed signal with the first delayed signal as the internal signal when the phase lock signal is activated and the command signal is not activated.

50. - 73. (Canceled)

74. (Currently Amended) A method of operating a delay locked loop, the method comprising:

generating multiple delayed signals by delaying an external clock signal;

selecting a first delayed signal among the multiple delayed signals to [[be]] generate an internal clock signal;

synchronizing the internal and external clock signals;

selecting a second delayed signal among the multiple delayed signals to [[be]] generate the internal clock signal when a command signal is activated while the external and internal clock signals are synchronized;

~~selecting~~ reselecting the first delayed signal to ~~be an~~ generate the internal clock signal when the command signal is deactivated; and

synchronizing the internal and external clock signals.

75. (Currently Amended) The method of claim 74 further includes selecting a third delayed signal among the multiple delayed signals to [[be]] generate the internal clock signal when another command signal is activated.

76. (Currently Amended) The method claim of 74, wherein generating ~~first and second~~ the multiple delayed signals includes applying unequal amount of delays to the external clock signal.

77. (Currently Amended) The method claim of 74, wherein selecting a first delayed ~~signals~~ signal includes selecting a signal that is generated by applying a first amount of delay to the external clock, wherein selecting a second delayed ~~signals~~ signal includes selecting a signal that is generated by applying a second amount of delay to the external clock signal, and wherein the first amount of delay is greater than the second amount of delay.

78. (Currently Amended) The method claim of 74, wherein selecting a first delayed ~~signals~~ signal includes selecting a signal that is generated by applying a first amount of delay to the external clock, wherein selecting a second delayed ~~signals~~ signal includes selecting a signal that is generated by applying a second amount of delay to the external clock signal, and wherein the first delay is smaller than the second amount of delay.

79. (Currently Amended) A method of operating a delay locked loop, the method comprising:

applying an amount of delay to an external clock signal to generate ~~an internal clock signal~~ a first delayed signal and a second delayed signal;

selecting a signal among the first and second delayed signals to generate an internal signal;

adjusting the amount of delay until the external and internal clock signals are synchronized; and

reducing the amount of delay by a delay quantity when a command signal is activated while the external and internal clock signals are synchronized and before the external and internal clock signals are detected as out of synchronism.

80. (Currently Amended) The method of claim 79 further includes:

increasing the amount of delay by the [[same]] delay quantity when the command signal is deactivated; and

adjusting the amount of delay until the external and internal clock signals are synchronized.

81. (Original) The method of claim 79, wherein reducing the amount of delay occurs before a phase detect signal is activated, wherein the phase detect signal is activated when the external and internal clock signal are not synchronized.

82. (Currently Amended) A method of operating a delay locked loop, the method comprising:

applying an amount of delay to an external clock signal to generate ~~an internal signal~~ a first delayed signal and a second delayed signal;

selecting a signal among the first and second delayed signals to generate an internal signal;

adjusting the amount of delay until the external and internal clock signals are synchronized; and

increasing the amount of delay by a delay quantity when a command signal is activated while the external and internal clock signals are synchronized and before the external and internal clock signals are detected as out of synchronism.

83. (Currently Amended) The method of claim 82 further includes:

reducing the amount of delay by the [[same]] delay quantity when the command signal is deactivated; and

adjusting the amount of delay until the external and internal clock signals are synchronized.

84. (Original) The method of claim 82, wherein increasing the amount of delay occurs before a phase detect signal is activated, wherein the phase detect signal is activated when the external and internal clock signal are not synchronized.